Microwave active devices and circuits fabrication technologies

Main Semiconductors Parameters

TABLE 3.1 Semiconductor Parameters at $T = 25°C$, $N \simeq 10^{16}\ cm^{-3}$

Parameter	GaAs	Si	Ge	GaAs 2 DEG
Electron mobility, μ_n ($cm^2/V \cdot s$)	5000	1300	3800	8000
Hole mobility, μ_p ($cm^2/V \cdot s$)	330	430	1800	—
Saturated drift velocity, v_s [cm/s (electrons)]	$1–2 \times 10^7$	0.7×10^7	0.6×10^7	$2–3 \times 10^7$
Band gap, E_g ($e \cdot V$)	1.42	1.12	0.66	—
Avalanche field, E_{max} (V/cm)	4.2×10^5	3.8×10^5	2.3×10^5	—
T_{max} (theory) [°C ($N \approx 10^{15}\ cm^{-3}$)]	500	270	100	—
T_{max} (practical)	350	200	75	—
Thermal conductivity, σ_T, at 150°C ($W/cm \cdot °C$)	0.30	1.0	0.40	0.30
σ_T at 25°C ($W/cm \cdot °C$)	0.45	1.4	0.60	0.45

Comparison between Silicon and GaAs

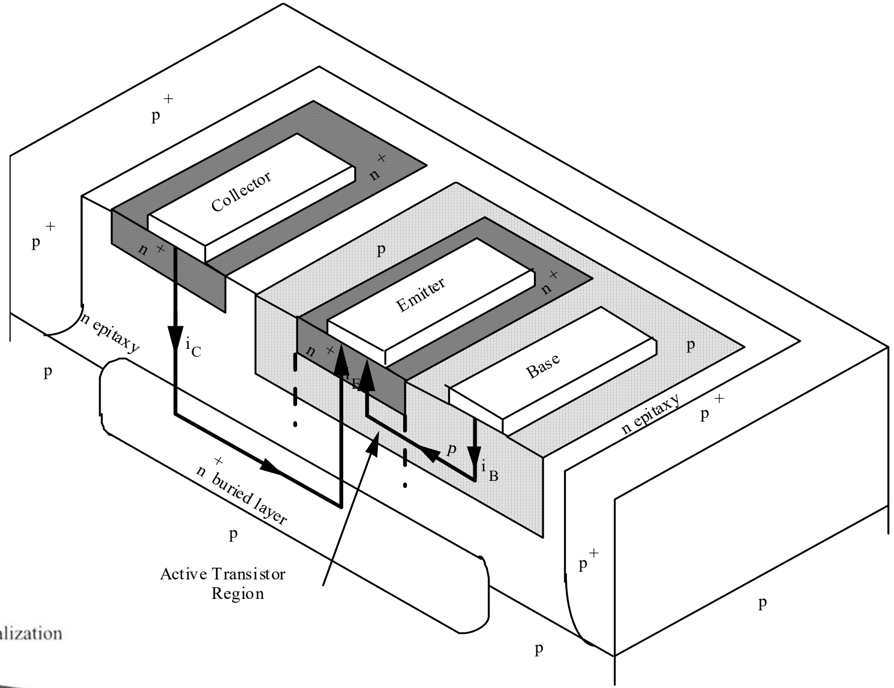
Pros of GaAs:

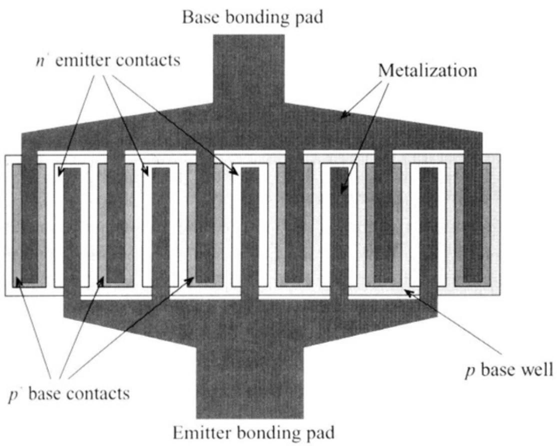
- Lower transit time of electric charge
- Higher max temperature (350° vs. 200°)
- Higher radiation resistance
- Substrate with higher resistivity (better intrinsic isolation, low parassitics)

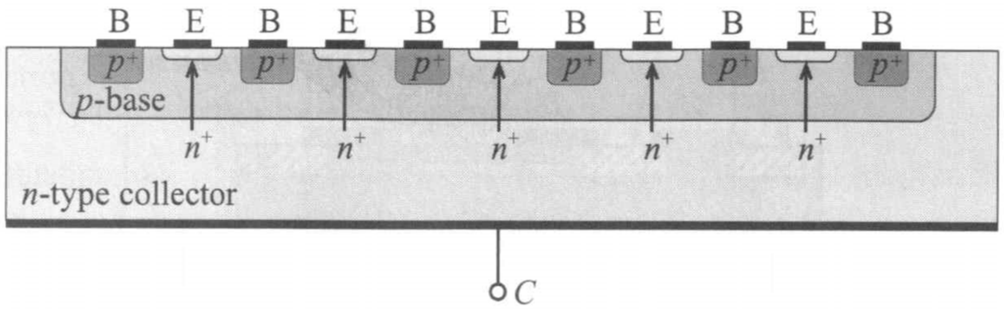
Cons of GaAs:

- Low mechanical robustness
- Low thermal conductivity
- Difficult to limit impurities (Not possible to fabricate good MOS devices)

Bipolar Transistors

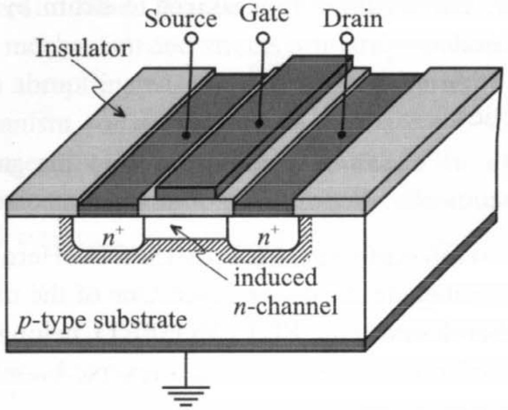




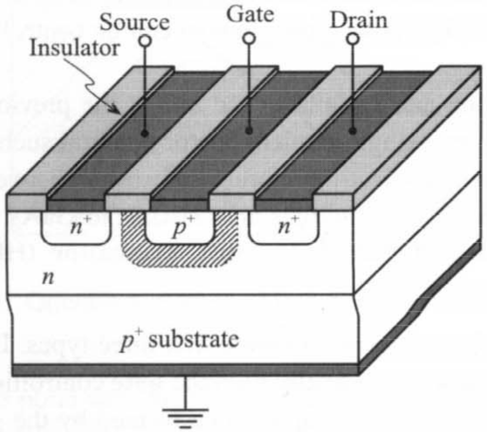


Power devices structure

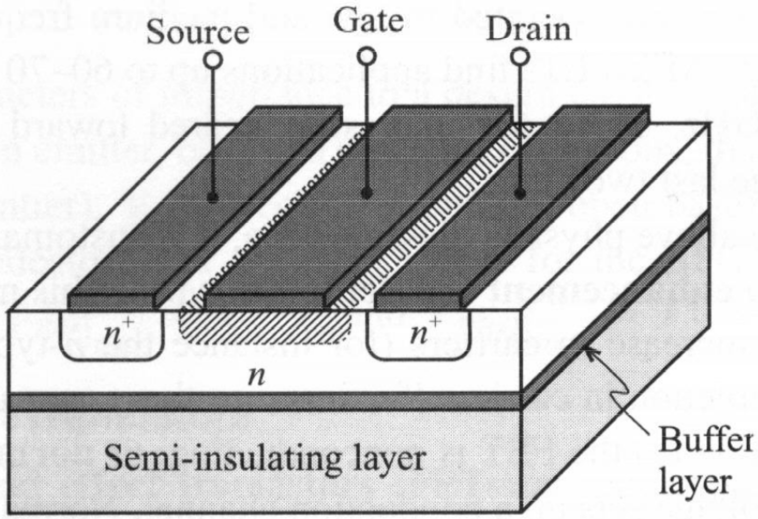
Unipolar Transistors



(a) Metal insulator semiconductor FET (MISFET)

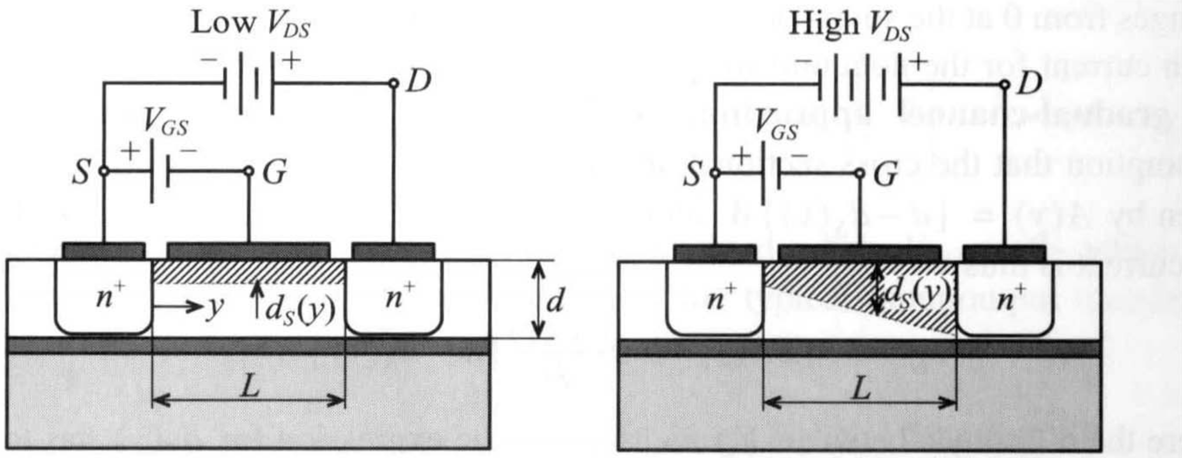


(b) Junction field effect transistor (JFET)



(c) Metal semiconductor FET (MESFET)

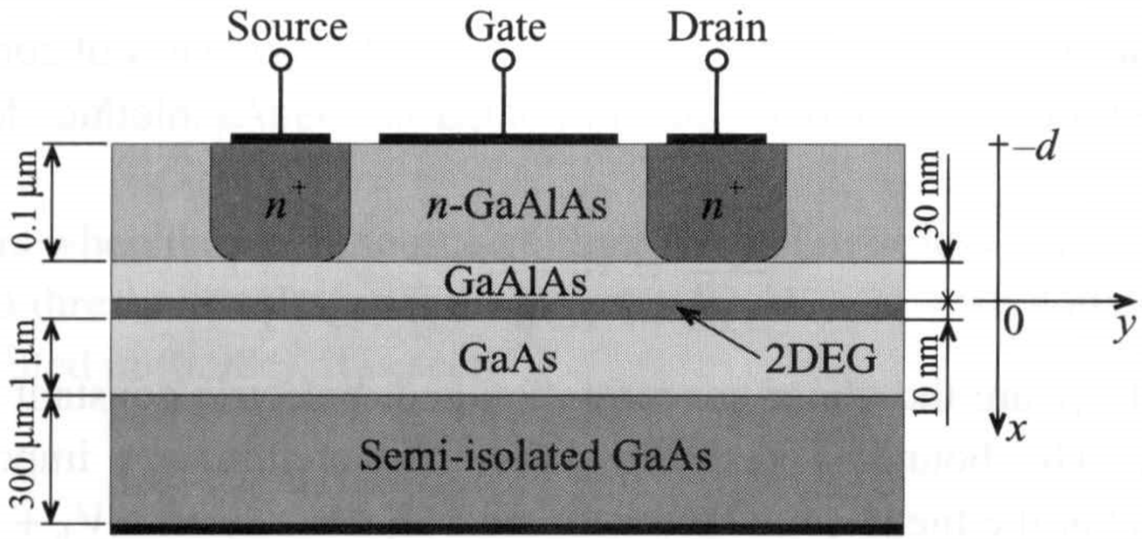
MESFET (Metal-Semiconductor gate)



(a) Operation in the linear region. (b) Operation in the saturation region.

- High carriers mobility → High current → high working frequency
- Key parameter: Channel length *L*
- It is possible to realize only *n* channel devices
- Intrinsic isolation (not doped substrate)

High Mobility Transistors (HEMT)



<u>Heterojunction</u>: junction between semiconductor with different band-gap (GaAlAs and GaAs in the figure)

The *n*-GaAlAs layer is used for realizing the gate MS junction

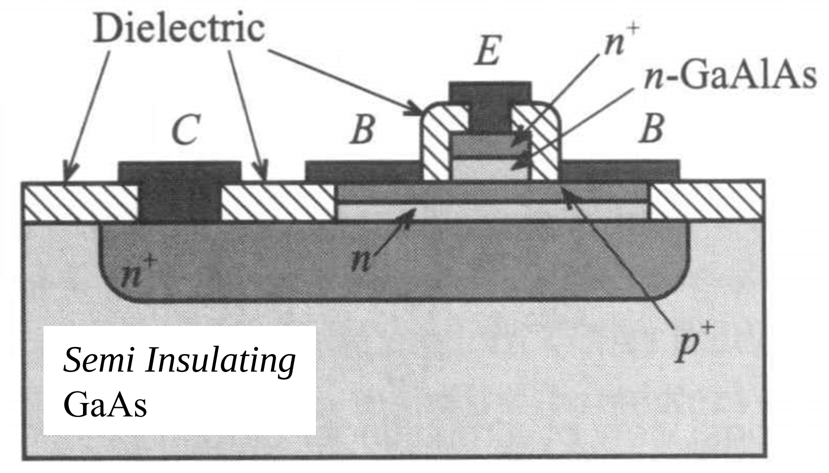
At the interface between GaAlAs and GaAs is generated a layer of electrons with a very high horizontal mobility (bi-dimensional gas).

The source-drain conductivity is controlled by the source-gate voltage (as in MESFETs)

Properties of HEMTs

- High electrons mobility in the bi-dimensional gas: 7000-8000 $cm^2v^{-1}s^{-1}$ vs. 5000 $cm^2v^{-1}s^{-1}$ in doped *n* GaAs
- The mobility even increases by refrigerating the device: at 77 °K we get 70000 $cm^2v^{-1}s^{-1}$. Also noise performances improve
- The drain-source channel is better confined with respect to MESFETs; as a consequence the small signal transconductance increases even for small values of drain current. Also the noise figure and the output conductance improve
- Recently the **pHEMT** (pseudomorphic HEMT) has been introduced. It is characterized by an additional layer of InGaAs between GaAs and GaAlAs. The maximum operating frequency is so further increased; also I_D current, for a given geometry and applied voltages, increases by a factor 2 with respect to a traditional HEMT

Heterojunction Bipolar Transistor (HBT)

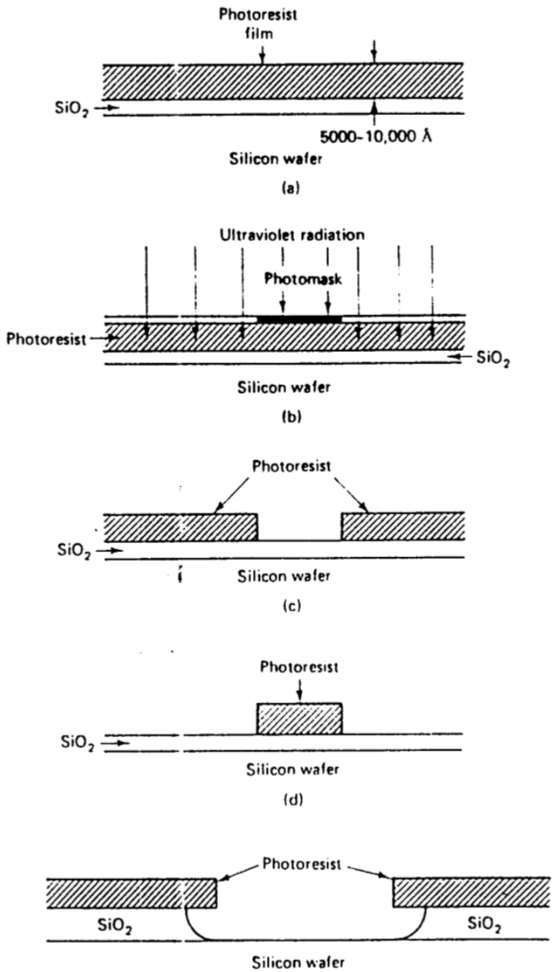


We can realize BJT operating at very high frequencies by means of GaAs heterojunction.
In the figure the junction base-emetter is realized betwee *p*-GaAs and *n*-GaAlAs. f_t increases because the transistor structure is vertical and the base length coincides with the p^+ epitassial layer thickness (typical dimensions: 10-20 nm)
With HBTs we can realize oscillators with low phase noise (corner frequency of *1/f* noise very close to zero)

Fabrication technologies of planar microwave circuits

- Traditional printed board:
  - Single dielectric layer (metallized at one side)
  - Active and passive discrete components (surface mount, via hole, etc.)
  - Interconnections, lines and distributed components realized through “printing”
- Integrated Circuits:
  - Hybrid Technologies (thick film, thin film, LTCC…)
  - Monolithic Technologies (MMIC on GaAs, SiGe…)
- Packaging
  - Modules inside metallic carrier
  - Case for integrated circuits (interconnections,…)

Photolithography: geometric patterns drawn on dielectric substrates



⇐A sensitive emulsion to ultraviolet light (*photoresist*) is deposited over a rigid substrate covered with SiO_2. The image of the pattern is generated on a photographic film (*photomask*)

⇐La photomask is placed over the photoresist and is exposed to ultraviolet light (photoresist is impressed)

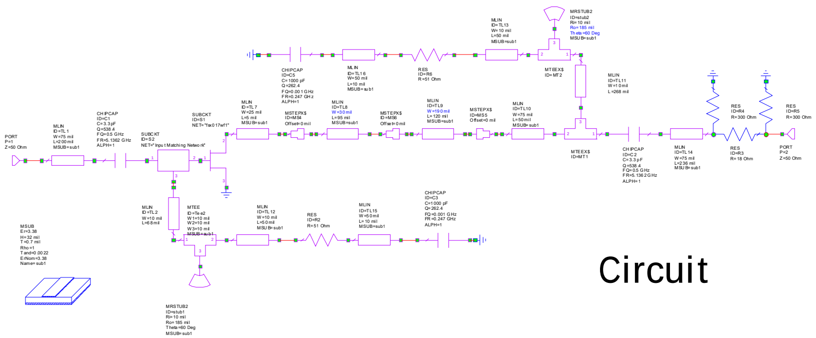
⇐Negative image: with a chemical etching the photoresist is removed where it is not impressed (in the end oxide is removed in correspondence of the pattern)

⇐Positive image: The impressed photoresist is removed (in the end oxide remains in correspondence of the pattern)

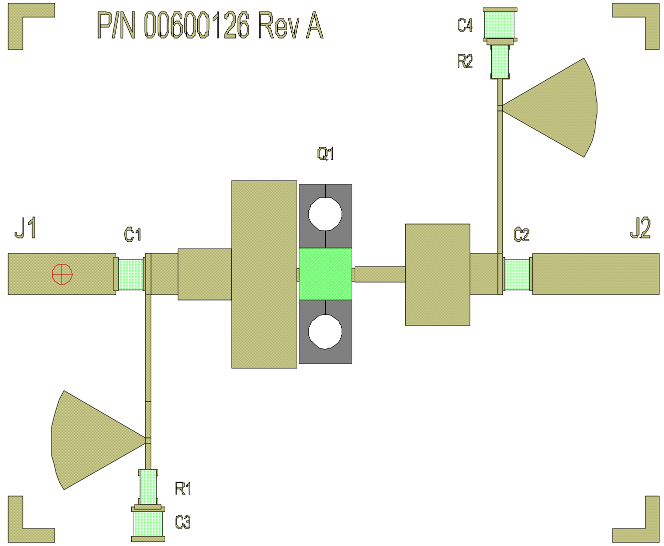
⇐With a suitable chemical solvent oxide is removed where it is not protected by the remaining photoresist

From the electrical circuit to the physical realization

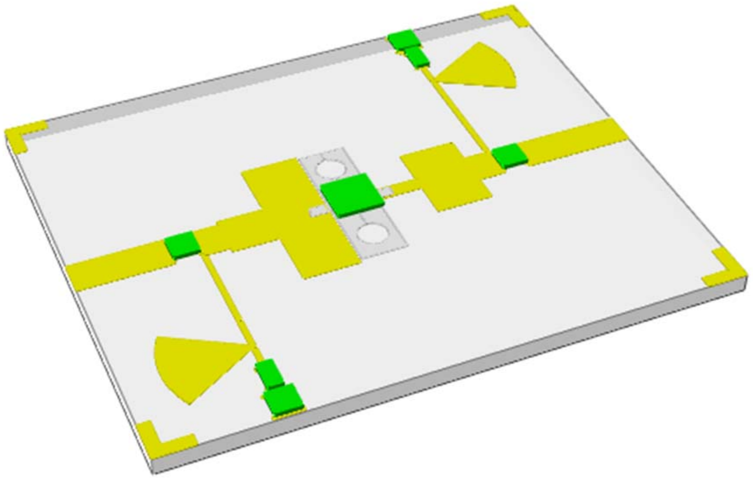
7 GHz Microwave FET Amplifier



Circuit



Layout (single layer)



Realization

Substrate: FR4

Conductor: Copper

Mask: Positive

Removal of excess cupper: through chemical solvent

Technological Limits of traditional printed board

- Minimum geometric dimensions limited by accuracy (typically 30-100 μm)
- Components density limited by the case size of discrete components
- Electromagnetic interactions between the circuit and the case (spurious resonances)
- Problems increase as the frequency becomes higher and higher

Hybrid integrated circuits

Hybrid integrations allows:

- To realize passive components with the same process used for the metallic patterns
- To employ active components without the case (→ size reduction)
- To increase the accuracy of the geometric pattern (Minimum dimensions of lines/gap 10-50 μm)
- To increase components density through the use of multilayer structures

“Thin Film” Integrated Circuits

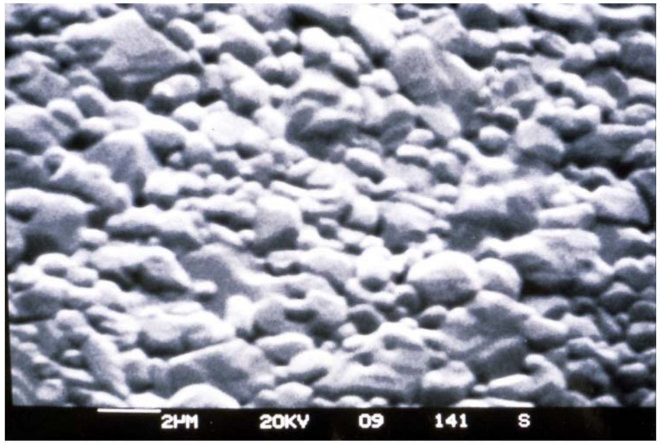
“Thin Film” refers to the material layers deposited on a substrate, generally insulant, with very small thickness (order of magnitude 0,1 μm). The property of the layers are strongly affected by the thickness as well as by the process characteristics of the layer deposition.

The “Thin Film” technology allows to integrate on the substrate:

- Conductive lines and microstrip
- Resistors
- Inductors
- Capacitors
- Cross-over

Substrate Characteristics

- Uniformity and anisotropy of dielectric constant
- Thickness uniformity
- Uniformity of surface roughness
- Mechanical robustness
- Thermal expansion coefficient (low)
- Thermal conductivity (good)



Common substrates materials

Common Substrates Materials and Their Applications

Material	Typical Users	Comments
Alimina (Al_2O_3) 99.6%	Low to medium power DC/RF or Microwave circuits using Si or GaAs Ics	Cost-effective material with wide range of applications
Beryllia (BeO)	High-power DC/RF/Microwave circuits using Silicol or GaAs Ics. High power terminations	Extremely high thermal conductivity
Aluminium-Nitride (AlN)	High-power DC/RFMicrowave circuits using silicon and GaAs ICs	Optimal CTE match with silicon devices
Quartz (SiO_2)	Microwave/millimeter-wave circuits requiring extremely low loss or loss CTE	Low Loss Tangent and GTE Smooth surface finish
Titanates	RF/Microwave amplifier or oscillators requiring High-Q resonators and transformers	Dielectric constants available from 12-100
Ferrite	RF/Microwave circulator/isolators	Magnetically activated material
Sapphire	Millimeter-wave/optical circuits with special electrical or mechanical requirements	Low Loss Tangent, Optical surface finish

Materials employed in thin film technology

Conductors:

- Gold (3-9 μm, galvanic)
- Palladium (2500 Å, sputtering)
- Titanium (500 Å, sputtering)

They increase the conductivity and guarantee adherence with the underlying layer

Resistors:

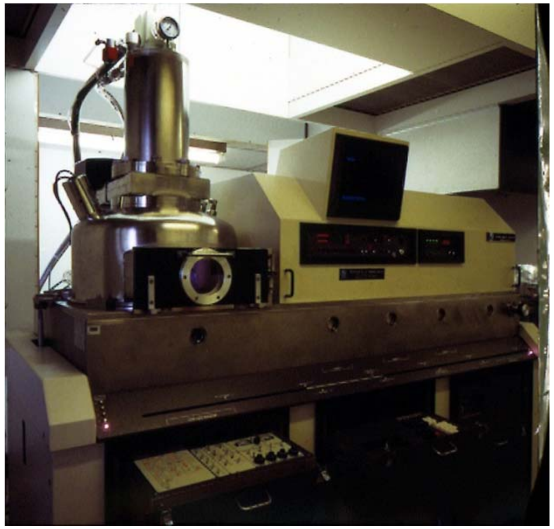
- Tantalum
- NiCr

Minimum dimensions of lines/gaps: 10-50 μm

Accuracy: 2-10 μm

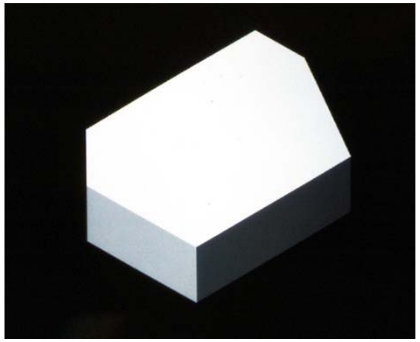
Film realization

Sputtering:
A plasma gas is created into a reactor starting from the material to be deposited (sputtered). The charged particles are accelerated and pushed against the substrate upon which are deposited creating the film (thickness 500-3000 A)

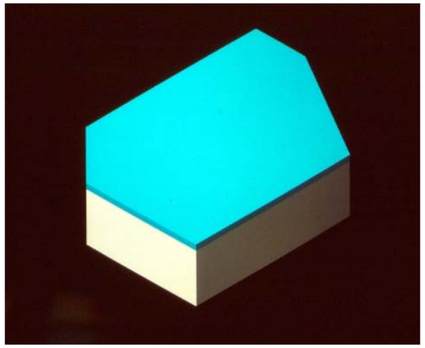


Electrochemical:
Growth through galvanic process.

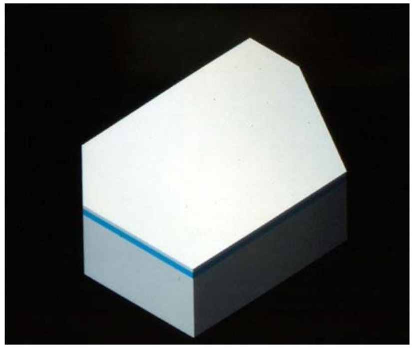
Fabrication of a thin film circuit (1)



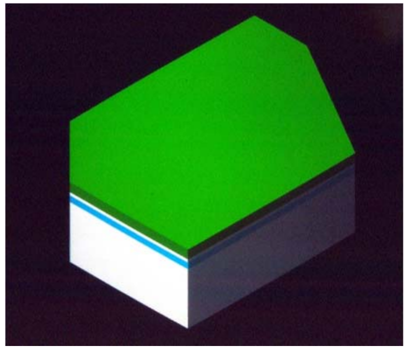
Substrate



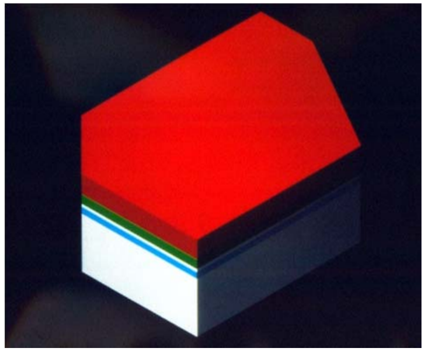
Tantalum Layer
(resistors)



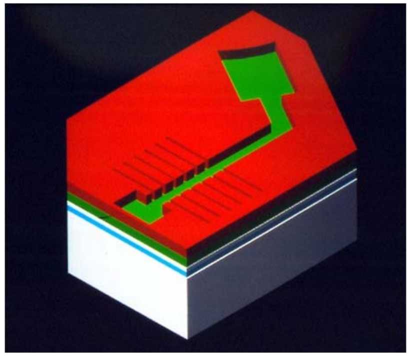
Titanium Layer
(conductors)



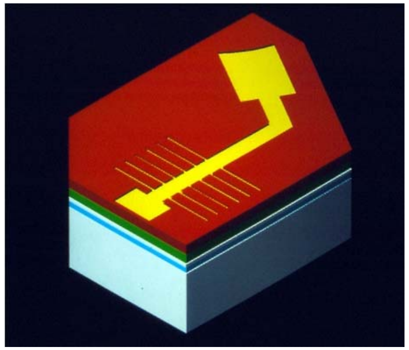
Palladium Layer
(adhesive)



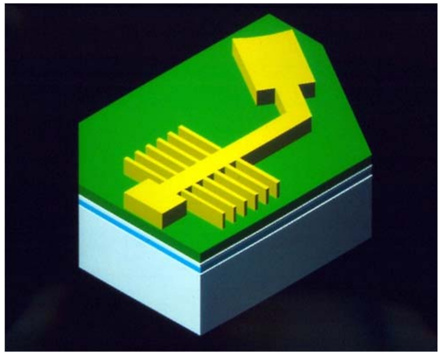
Photoresist



Conductor Pattern
+ resistors

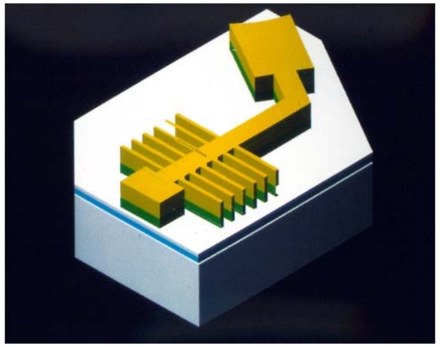


Gold deposition
(galvanic)

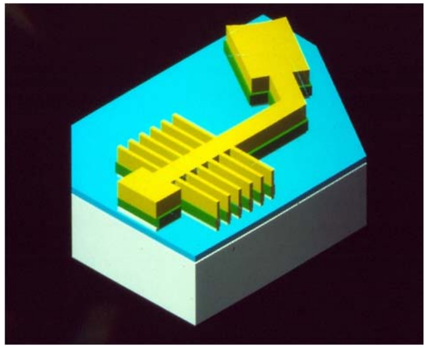


Photoresist removal

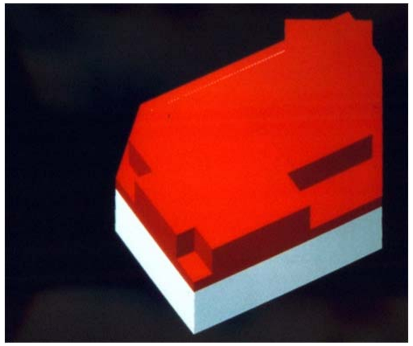
Fabrication of a thin film circuit(2)



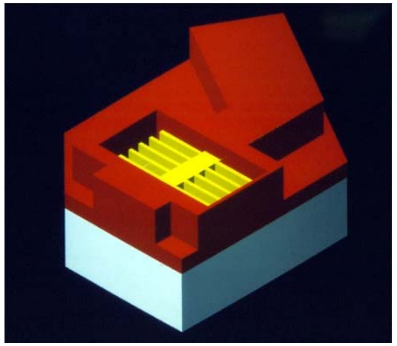
Palladium removal



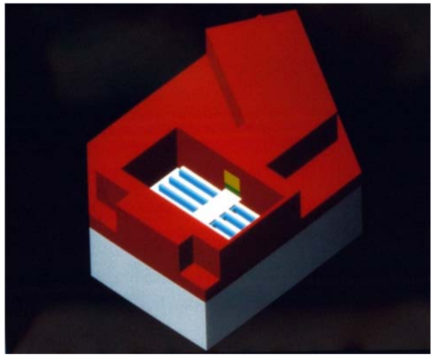
Titanium removal + Gold galvanic growth



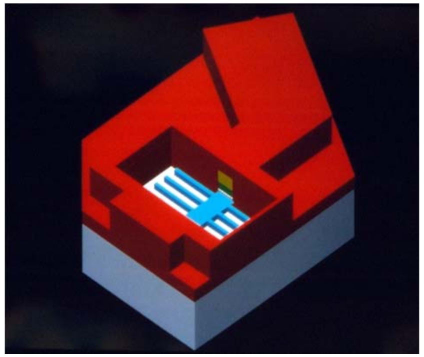
Photoresist coating



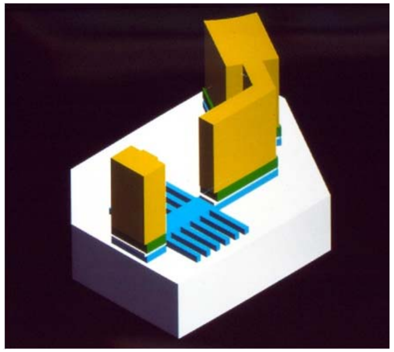
Resistor Pattern



Gold + Palladium removal



Titanium removal



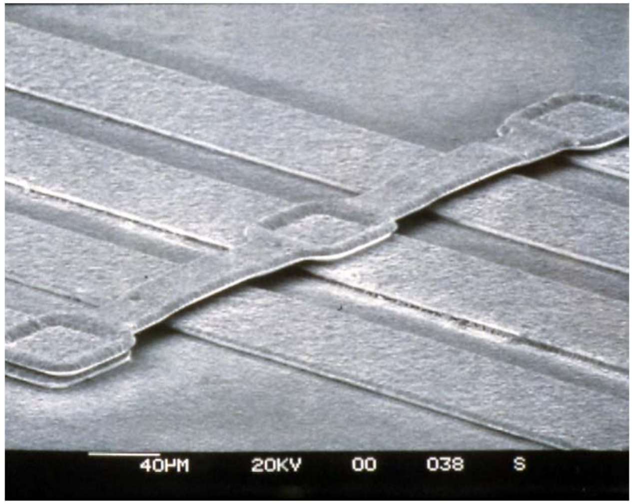
Photoresist removal

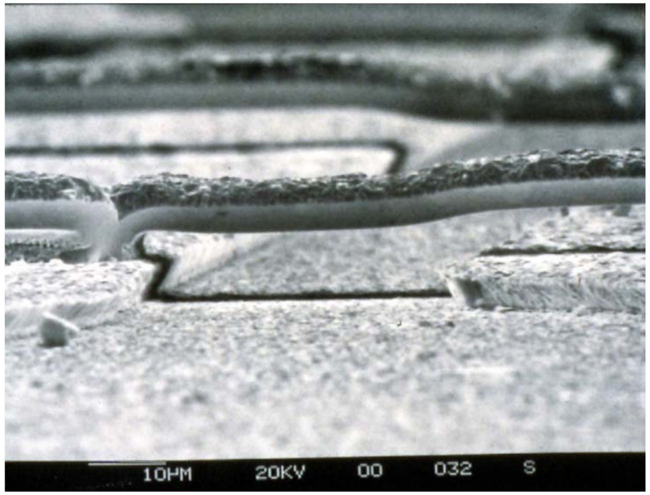
Machining

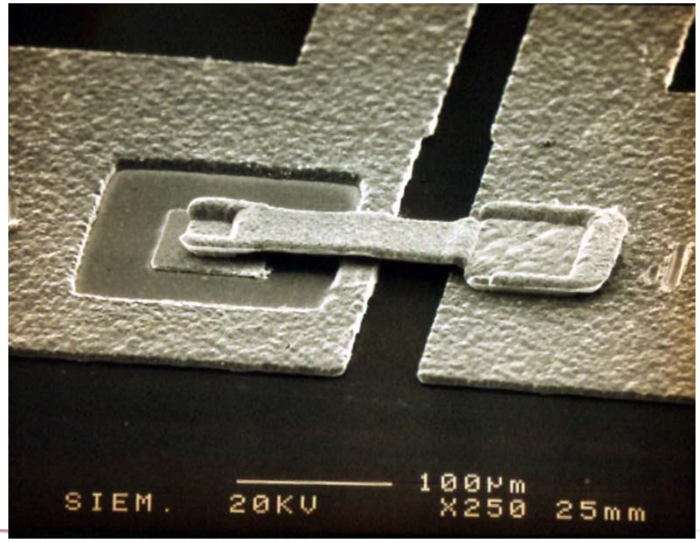
Via hole: Realization of a inner metalized hole (gold). Via holes belong to conductive layers; the hole in the substrate is realized by a laser before the conductive layers suttering

Substrate drilling: it is requested also for fixing the circuit in the case (through screws). It is realized with a laser o ultrasonic drill after the circuit realization

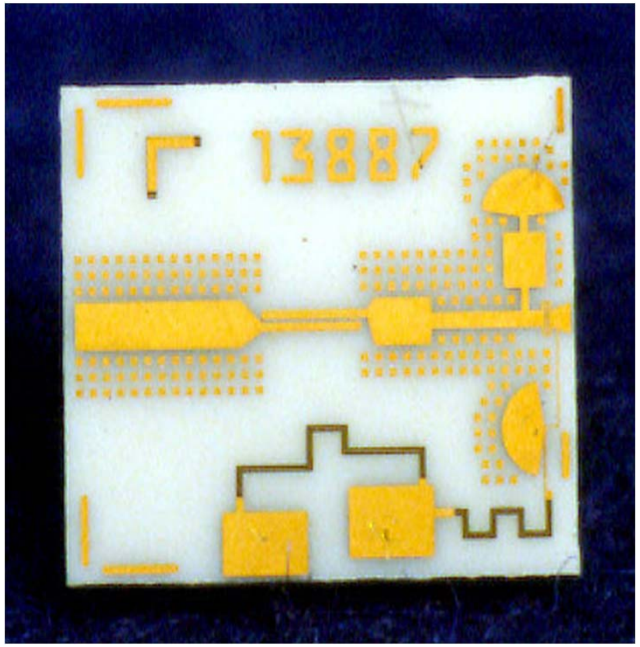
Other components: air bridges

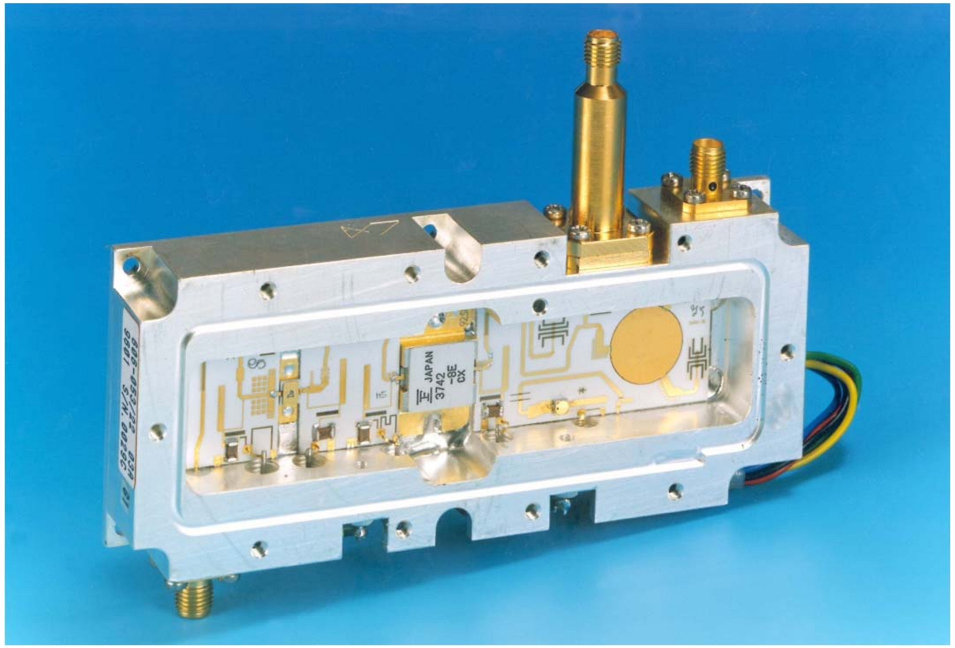






Examples





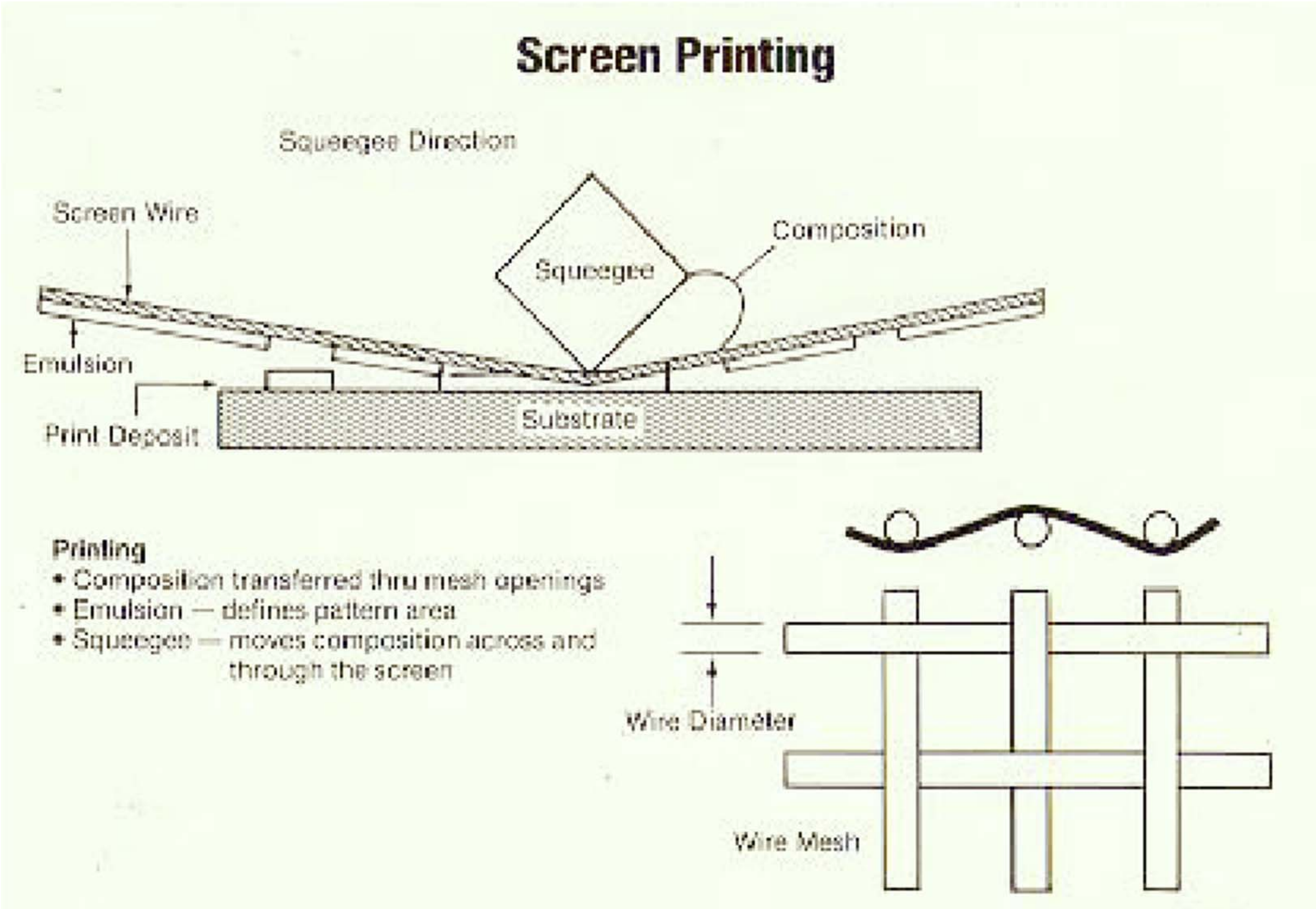
“Thick Film” circuits

This technology is more convenient (less expensive) with respect the thin film when a lower accuracy is requested (and the production volume is smaller)

General features:

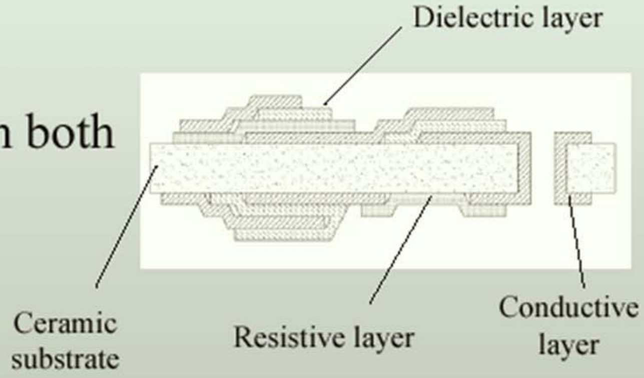
- Minimum dimensions: 50-100 μm
- Accuracy: 10-50 μm
- Pattern transferred on a wire screen mesh
- Substrates: similar to thin film technology
- Materials:
  - Conductors: Gold, copper, silver
  - Resistors: special mixture of resins
- Multi layers circuits possible

Realization of a thick film circuit



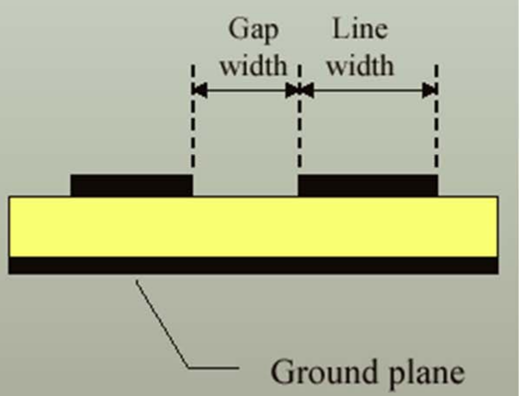
Possibilities of thick film

Multilayer (front/back):
by adding successive layers of mixed materials on both sides of the ceramic substrate, package density is increased and shielding can be improved.



Screen printing accuracy:
Gold-based materials allow a line/gap width of 100µm, with a tolerance of ±10µm.
Comparison with dimensions obtainable with other technologies (at similar yields):

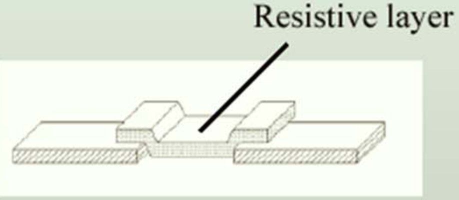
- Fodel/Green Tape: down to 50µm;
- Thin Film: down to 25µm;
- Standard production PCBs: down to 200±30µm.



Basic Components

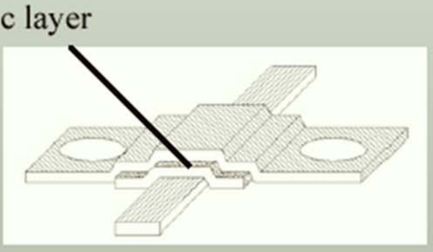
Resistors:

- From few Ω to several MΩ, using different resistive layers (10 Ω/□ to 1 M Ω/□);
- Low to high power ratings;
- Laser trimming to ± 0.5 % tolerance.



Capacitors:

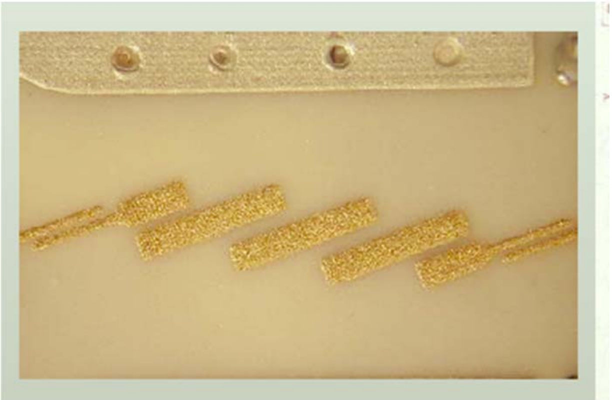
- Single layer, multilayer and feedthrough capacitors;
- Tolerances not better than ±30%.



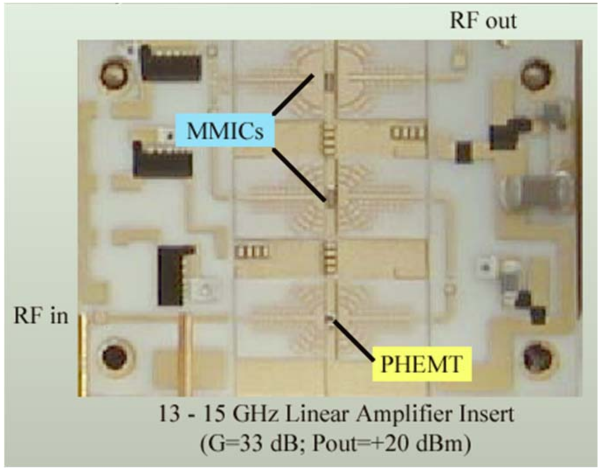
Inductors:

- Microwave spiral inductors, and UHF coils;
- Up to 100 nH, with Q up to 90.

Examples of thick film circuits



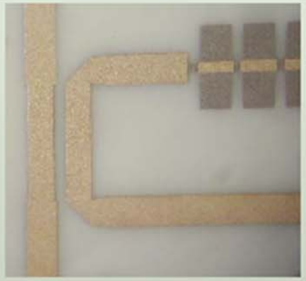
Filtro a 38 GHz “Edge-coupled”



Amplificatore lineare 13-15 GHz

“Twisted line” hybrid splitter

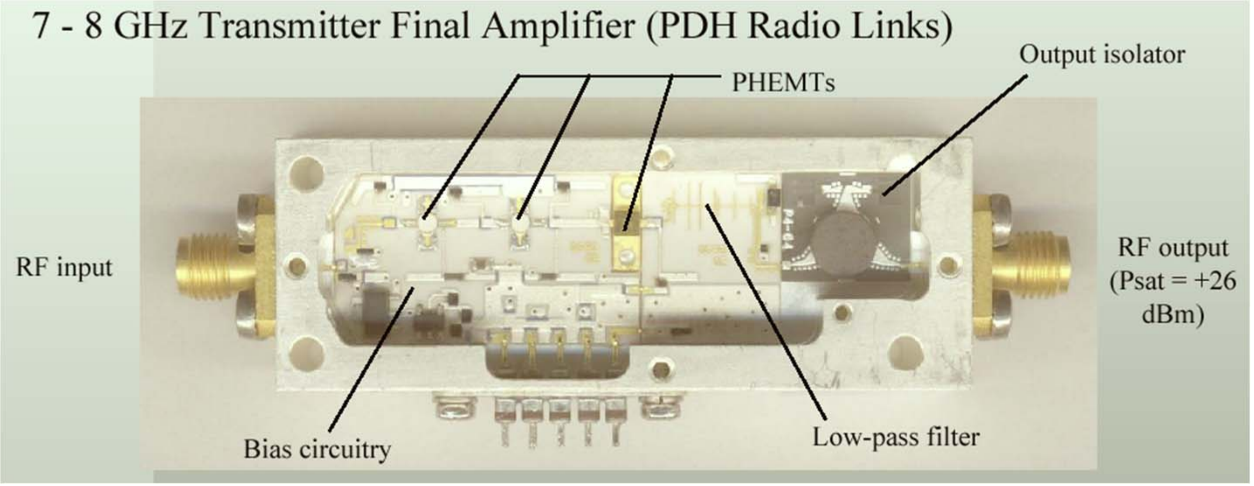
Branch line coupler

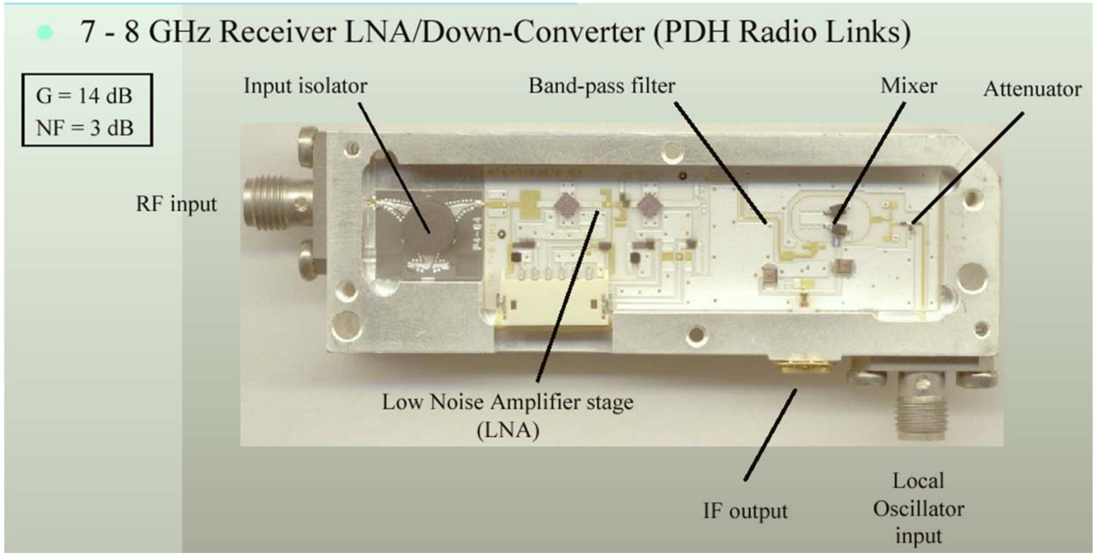


Directional coupler, with distributed termination

Directional coupler, with grounded termination and RF detector

Examples of complete systems



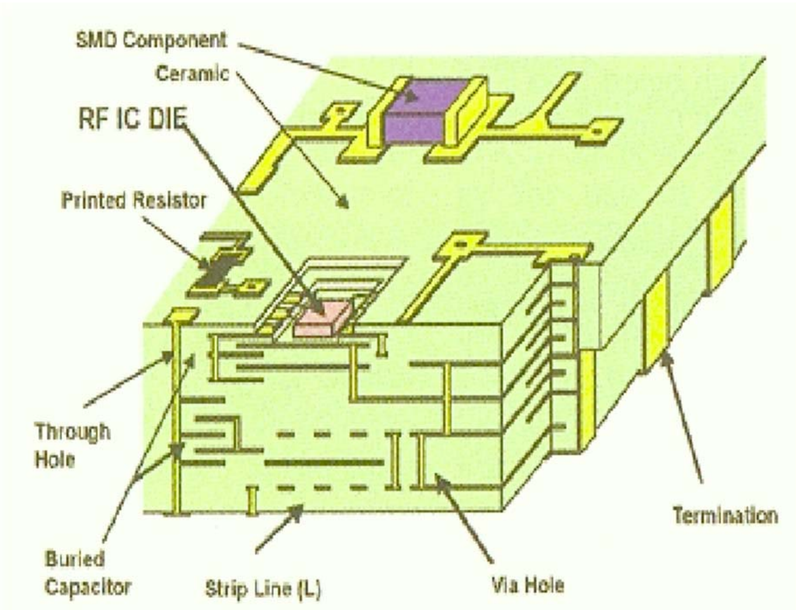


LTCC Technology (notes)

“LTCC” is an acronym for:

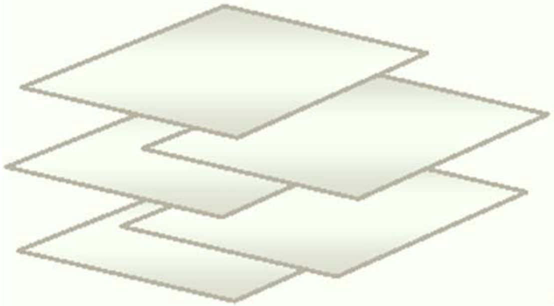
Low Temperature Co-fired Ceramic

With this integration technology is possible realize multi-layer extremely compact structures with passive components. Active components can be added on the top and bottom layers

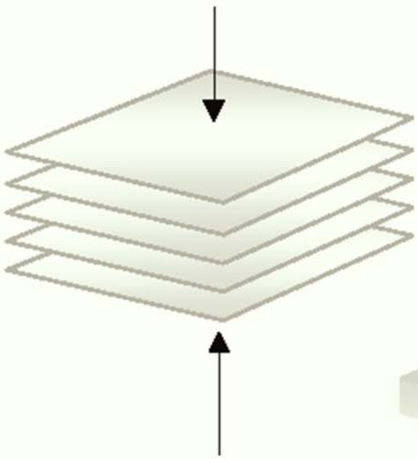


Realization of LTCC circuits

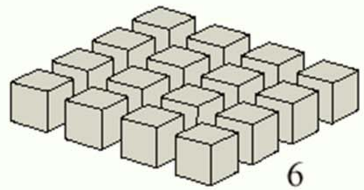
- Individual Tape layers are prepared by forming and filling vias.
- Signal, power and ground are applied by screen printing
- Fine line geometries made be applied utilizing co-fired Fodel®
- Passive devices may be applied in the form of high K paste or tape, co-fired resistors and inductors.



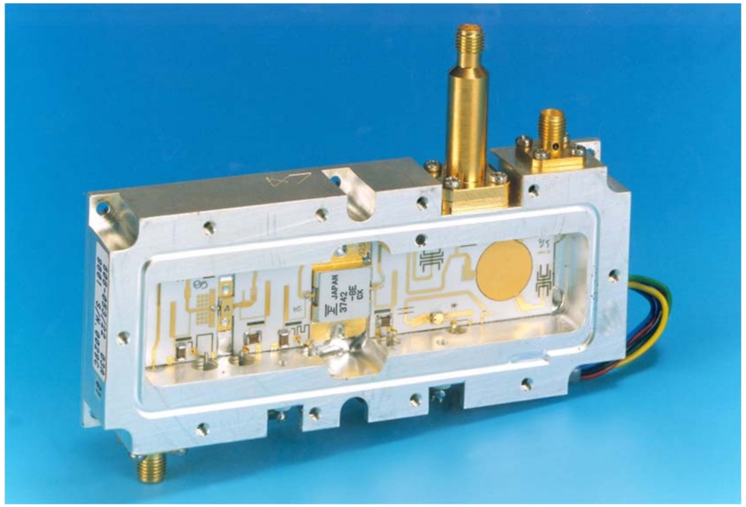
- Individual layers are then collated using a precision tooling fixture and laminated at 3000 PSI



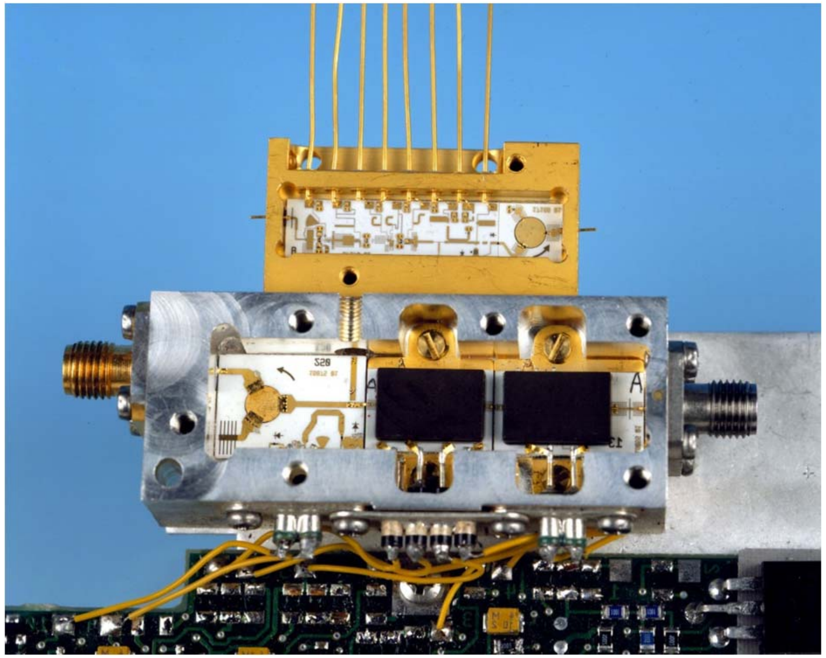
- The laminate is then fired at 850° C
- Individual circuits may be singulated prior to firing or directly after



Packaging of microwave circuits



Traditional solution:
The circuit is inserted into a metallic container (carrier)



Innovative solution
"Chip & Wire" Technology : carrier of compact dimensions; wired external connections. Suitable for chip components (without case)